CLAIMS

1. A design support apparatus for semiconductor devices that supports wiring design for bond wires that connect a semiconductor chip and an interposer, the design support apparatus for semiconductor devices comprising:

a unit that creates simulated design data simulating occurrence of fluctuation in an arrangement position of a semiconductor chip on an interposer and occurrence of fluctuation in bond wire connection terminal positions of the interposer; and

an analyzing unit that analyzes, based on the simulated design data, deficiencies in manufacturing of semiconductor devices due to the fluctuation in the arrangement position of the semiconductor chip on the interposer and the fluctuation in the bond wire connection terminal positions of the interposer.

2. The design support apparatus for semiconductor devices that supports wiring design for bond wires that connect a semiconductor chip and an interposer according to claim 1, the design support apparatus for semiconductor devices comprising:

a unit that creates simulated design data simulating occurrence of fluctuation in an arrangement position of a semiconductor chip on an interposer and occurrence of fluctuation in bond wire connection terminal positions of the interposer; and

an analyzing unit that analyzes, based on the simulated design data, a tolerance of the fluctuation in the arrangement position of the semiconductor chip on the interposer and a tolerance of the fluctuation in the bond wire connection terminal positions of the interposer.

3. A design support apparatus for semiconductor devices comprising:

a first data creating unit that creates, based on design data of a semiconductor package, semiconductor chip simulated arrangement data obtained by arranging a semiconductor chip in a position where fluctuation in an arrangement position of the semiconductor chip in arranging the semiconductor chip on an interposer is simulated;

a second data creating unit that creates, based on the design data of the semiconductor package and the semiconductor chip simulated arrangement data, bond wire simulation data obtained by wiring, using bond wires, the bond wire connection terminals of the semiconductor chip arranged to deviate from an arrangement position in the design data and bond wire connection terminals of the interposer;

a measuring unit that measures a design rule for the bond wires used for the wiring from the bond wire simulation data; and

an analyzing unit that performs analysis of a measurement result in the measuring unit.

4. The design support apparatus for semiconductor devices according to claim 3, wherein, as the design data of the semiconductor package, a shape of the interposer, a shape of the semiconductor chip, an arrangement position of the semiconductor chip on the interposer, a shape of the bond wires that connect the semiconductor chip and the interposer, and arrangement positions of the bond wires that connect the semiconductor chip and the interposer are used.

5. The design support apparatus for semiconductor devices

according to claim 3, wherein the first data creating unit creates semiconductor chip simulated arrangement data obtained by arranging, with respect to the arrangement position of the semiconductor chip on the interposer in the design data of the semiconductor package, the semiconductor chip in a position where fluctuation in an arrangement position of the semiconductor chip in an in-plane direction or a rotation direction on a semiconductor chip arrangement surface of the interposer or fluctuation in inclination of the semiconductor chip in a thickness direction of the interposer is simulated.

6. The design support apparatus for semiconductor devices according to claim 3, wherein the measuring unit measures clearance among the bond wires and clearance between the bond wires and the semiconductor chip as a design rule for the bond wires used for wiring.

7. The design support apparatus for semiconductor devices according to claim 6, wherein the analyzing unit analyzes a tolerance of fluctuation in an arrangement position of the semiconductor ship on the interposer that satisfies the design rule.

8. The design support apparatus for semiconductor devices according to claim 6, wherein the analyzing unit analyzes a tolerance of fluctuation in bond wire connection terminal positions of the interposer that satisfies the design rule.

9. The design support apparatus for semiconductor devices according to claim 3, comprising a storing unit that stores the measurement result in the measuring unit.

10. The design support apparatus for semiconductor devices according to claim 3, comprising a storing unit that stores an analysis result in the analyzing unit.